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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,949	LEVY ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-23,25-27 and 30-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-34* is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-17,19-23,25 and 27* is/are rejected.

7)☒ Claim(s) *9,18,26,35,36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-8, 10, 13-17, 19, 20, 23, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Bernstein et al. (U. S. PAT. 6,794,901).

In claim 1, Bernstein et al. teaches all claimed features in Fig. 2, a keeper circuit for a dynamic node (PCN) of a circuit, wherein the effective strength (the amount of charge; col. 3, line 64) of the keeper circuit (210) operating on the dynamic node is reduced from a non-zero strength level (when EI signal from 215 is a logic 0) to a second non-zero strength level (when EI signal is a logic 1) during an interval (an interval when T13 and T12 supply the same amount of charge to when T13 supplies less charge than T12) in which at least one path in an evaluation circuit (T8-T10) is sensitive to a keeper device (T13) and wherein the effective strength of the keeper circuit operating in a dynamic node (PCN) is restored to the first non-zero strength after arrival of a latest signal transitioning to a level (instant before PC signal ready for transitioning from logic 1 to logic 0; instant before T11 ceases to conduct) that can discharge the dynamic node.

In claims 2-3, Bernstein et al. further teaches the circuit of claim 2, wherein the sensitivity of the at least one path includes output of an incorrect value of the evaluation circuit output (noise); wherein a response to the sensitivity is otherwise a reduced speed of the evaluation circuit output (reducing soft errors).

In claim 5, Bernstein et al. teaches all claimed features in Fig. 2, a circuit comprising: a dynamic node (PCN); an evaluation circuit (T8-T10) coupled to the dynamic node; a keeper circuit (210) coupled to the dynamic node (PCN) wherein the keeper circuit has a first non-zero strength (when EI signal from 215 is a logic 0) during a first interval (an interval when T13 and T12 supply the same amount of charge) and a second non-zero strength (when EI signal is a logic 1) during a second interval (an interval when T13 supplies less charge than T12), the first non-zero strength being substantially greater than the second non-zero strength (the same amount of charge supplied by both T13 and T12 is greater than the charge supplied by T13 and T12 when T13 supplies less charge than T12); and wherein the first interval begins before arrival of an earliest signal transitioning (instant before PC signal transitioning from a logic low to a logic 1; when T11 is starting to conduct) to a level that can discharge the dynamic node; and wherein the second interval begins after arrival of a latest signal transitioning (instant before PC signal transitioning from logic 1 to logic 0 again; instant before T11 ceases to conduct) to a level that can discharge the dynamic node.

In claims 6-8, Bernstein et al. further teaches the circuit of claim 5, wherein the keeper circuit (210) latches an output (Z) of the circuit; and wherein the keeper circuit includes a first keeper device (T13); and when the keeper circuit includes a keeper

gating device (T14) coupled to the first keeper device (T13) and the dynamic node (PCN).

In claim 10, Bernstein et al. further teaches the circuit of claim 5, wherein the keeper is responsive to a keeper control (EI signal from 215).

In claim 13, Bernstein et al. further teaches the circuit of claim 5, comprising: a clock node (PC); a precharge device (T7) couple to the clock node and the dynamic node (PCN); and a discharge device (T11) coupled to the clock node and the evaluation circuit (T8-T10).

In claim 14, Bernstein et al. further teaches the circuit of claim 13, wherein the precharge device (T7) and the evaluation circuit (T8-T10) operates during different phases (inherent) of a control signal (PC).

In claim 15, Bernstein et al. further teaches the circuit of claim 7, wherein the first keeper device is sized to sufficiently overcome the leakage current in the evaluation circuit (inherent).

In claim 16, Bernstein et al. further teaches the circuit of claim 5, wherein a reduction in the effective strength of the keeper circuit from the first non-zero strength to the second non-zero strength occurs before arrival of an earliest signal (at the start of PC signal transitioning from logic 0 to logic1) transitioning to a level that can discharge the dynamic node.

In claim 17, Bernstein et al. further teaches the circuit of claim 5, wherein the effective keeper circuit strength is restored to the first non-zero strength from the second non-zero strength after arrival of a latest signal transitioning to a level (instant

before PC signal ready for transitioning from logic 1 to logic 0) that can discharge the dynamic node.

In claim 19, Bernstein et al. further teaches the circuit of claim 5, wherein the dynamic node (PCN) is precharged high (VDD).

In claim 20, Bernstein et al. further teaches the circuit of claim 19, wherein the evaluation circuit is n-logic (T8-T10 are nMOS).

In claim 23, Bernstein et al. teaches all claimed features in Fig. 2, a method for evaluating a dynamic node, comprising: precharge a dynamic node (PCN); effectively disabling a first keeper device (T13 is off when EI signal at the gate of T14 is a logic 1) coupled to the dynamic node during an interval (an interval when T13 and T12 supply the same amount of charge to when T13 supplies less charge than T12) in which at least one path in an evaluation circuit (T8-T10) is sensitive to a keeper device (210); evaluating an evaluation circuit (when PC signal is a logic 1); protecting the dynamic node from noise (soft errors) during the interval; and effectively enabling (when EI signal at the gate of T14 is a logic 0, T13 is turned on) the first keeper device after arrival of a latest signal transitioning to a level (instant before PC signal ready for transitioning from logic 1 to logic 0; instant before T11 ceases to conduct) that can discharge the dynamic node (PCN).

Claim 25 corresponds to detailed circuitry already discussed similarly with regard to claim 1.

Claim 27 corresponds to detailed circuitry already discussed similarly with regard to claim 23.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bernstein et al.

In claim 11 Bernstein et al. teaches all claimed features the circuit of claim 10; with the exception of the keeper control is clock. However, controlling the keeper control with signals other than EI signal is well known in the art because the keeper control of Bernstein et al. can accept signals other than EI signal.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to control the keeper control with clock signal, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In Re Leshin*, 125 USPQ 416.

Claim 12 is rejected in the same manner.

5. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bernstein et al. in view of Karnik et al. (U. S. PAT. 6,366,132).

In claim 21, Bernstein et al. teaches all claimed features the circuit of claim 5; with the exception of teaching wherein the dynamic node is precharged low. However,

Karnik et al. teaches in Fig. 9, a dynamic node (N50) is precharged low (when T44 is closed).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to precharge the dynamic node of Bernstein's circuit to low level or ground, in order to provide another version of Bernstein's circuit.

In claim 22, Bernstein et al. teaches all claimed features the circuit of claim 5; with the exception of teaching wherein the evaluation circuit is p-logic. However, Karnik et al. teaches in Fig. 9, the evaluation circuit (94) is p-logic (P-stack).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select p-logic in lieu of n-logic, in order to provide another version of Bernstein s circuit.

6. Claims 9, 18, 26, 35 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 30-34 appear to comprise allowable subject matter.

Response to Arguments

8. Applicant's arguments filed 10/07/2005 have been fully considered but they are not persuasive.

Regarding amended claim 1, the Examiner respectfully believes the prior art of Bernstein et al. in Fig. 2 teaches all claimed recitations, which also includes the newly added recitation of after arrival of a latest signal transitioning to a level that can discharge the dynamic node. *The latest signal transitioning is the instant before PC*

signal ready for transitioning from logic 1 to logic 0 which is the instant before T11 ceases to conduct.

Regarding amended claim 5, Bernstein et al. in Fig. 2 further teaches the newly added recitations of wherein the first interval begins before arrival of an earliest signal transitioning to a level that can discharge the dynamic node and wherein the second interval begins after arrival of a latest signal transitioning to a level that can discharge the dynamic node. The Examiner believes *the first interval begins the instant before PC signal transitioning from logic 0 to logic 1 and when T11 starts to conduct (closed) and the second interval begins the instant before PC signal transitioning from logic 1 to logic 0 again, before T11 ceases to conduct to the level that the node PCN can be discharged.*

The newly recited limitations of claim 23 are explained in the above detailed action.

Claim 25 corresponds to claim 1 and claim 27 corresponds to claim 23.

The rejection of claims 1-3, 5-8, 10-17, 19-23, 25 and 27 is maintained.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER